

REMARKS

This is intended as a full and complete response to the Office Action dated April 19, 2004, having a shortened statutory period for response set to expire on July 19, 2004. Claims 1-27 are pending in the application and remain pending following entry of this response. Please reconsider the claims pending in the application for reasons discussed below.

Claim Rejections 35 USC §102

Claims 1-2, 22, 24, 25, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by *Katoh* (U.S. Patent No. 6,252,465).

With respect to claims 1 and 22, the Examiner states *Katoh* discloses, in Figure 3, a phase blending circuit and a corresponding method for generating a plurality of signals differing in phase relative to an early phase signal comprising a) a current source [top transistor of box 28] having a common output node [common node of drains of transistors in box 28]; b) one or more delay elements [inverter in box 27], and c) one or more switches [first and bottom transistors of box 27] to selectively couple one or more of the delay elements to the common output node of the current source, wherein a time required for a voltage level at the common output node to fall below a threshold level after assertion of the early phase signal is dependent on which of the one or more delay elements are coupled to the common output node.

Applicants respectfully submit, however, that the one or more delay elements disclosed in Figure 3 of *Katoh* are not selectively coupled to the common output node of the current source via the one or more switches, as claimed. In contrast, only transistors of the output element (stage 28) are coupled (and not selectively) to the common output node of the current source (as correctly stated in the Office Action). Further, each delay element (stage 27) is coupled to its own current source(s) via top and bottom transistors, while the output of each delay element 27 is coupled to the input of the next delay element 27 (or output element 28). Rather than control the overall delay of the DLL circuit via selective coupling of delay elements, as claimed, *Katoh* teaches controlling the delay of each delay element commonly, with each delay element

27 receiving the same current control signals from a current control circuit 25 (see col. 8, lines 51-57).

Accordingly, Applicants respectfully request withdrawal of this rejection.

Claim Rejections - 35 USC § 103

Claims 5-7 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Katoh* in view of *Saeki* (U.S. Patent No. 6,388,490).

Applicants submit, however, that *Katoh* has been overcome with respect to claims 1 and 22 for reasons stated above. As claims 5-7 and 26 each depend from claims 1 or 22, and contain all the limiting features thereof, Applicants also submit that these claims are patentable over *Katoh* and *Saeki*, and respectfully request withdrawal of this rejection.

Claims 14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (Fig. 1) in view of *Katoh*.

The Examiner relies on Fig. 1 of the present application as disclosing all of the elements of claim 14, except the claimed phase blending circuit. However, the Examiner cites *Katoh* as disclosing the elements of the claimed phase blending circuit. For reasons described above, however, Applicants submit that rather than teaching a phase blending circuit that selectively couples delay elements to a common output node of a current source, as claimed, *Katoh* teaches a circuit that controls the delay of a plurality of delay elements commonly, with each delay element 27 receiving the same current control signals from a current control circuit 25. Therefore, Applicants submit that, even if combined as suggested in the Office Action, the teachings of the prior art FIG. 1 and *Katoh* do not teach all the elements of claim 14.

Accordingly, Applicants submit that claim 14 and its dependent claims 16 and 17 are patentable over the teachings of FIG. 1 and *Katoh* and respectfully request withdrawal of this rejection.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Kwak* (U.S. Patent No. 6,646,939) in view of Applicants' Admitted Prior Art (Fig. 1) and *Katoh*.

PATENT

Infineon Dkt. No.: 2003P52879US

OC Docket No.: INFN/0026

With respect to claim 18, the Examiner relies on *Kwak* as disclosing a dynamic random access memory (DRAM) device comprising a) one or more memory elements [60,70]; and b) a delay locked loop circuit [20] for synchronizing data output from the one or more memory elements with a clock signal. While the Examiner states that *Kwak* fails to disclose a detailed description of the claimed delay locked loop, the Examiner submits that this description is provided by combination of FIG. 1 of the current application and *Katoh*. For reasons described above, however, Applicants submit that rather than teaching a circuit that selectively coupling delay elements to a common output node of a current source, as claimed, *Katoh* teaches a circuit that controls the delay of a plurality of delay elements commonly, with each delay element 27 receiving the same current control signals from a current control circuit 25.

Therefore, Applicants submit that, even if combined as suggested in the Office Action, *Kwak*, the prior art FIG. 1, and *Katoh* do not teach all the elements of claim 18. Accordingly, Applicants respectfully request withdrawal of this rejection.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Kwak* in view of Applicants' Admitted Prior Art (Fig. 1) and in view of *Katoh* and further in view of *Saeki*.

Applicants submit, however, that *Kwak*, the prior art FIG. 1 and *Katoh* have been overcome with respect to claim 18 for reasons stated above. As claim 20 depends from claim 18, and contains all the limiting features thereof, Applicants also submit that this claim is patentable over *Kwak*, the prior art FIG. 1, *Katoh*, and *Saeki*, and respectfully request withdrawal of this rejection.

Allowable Subject Matter

Applicants acknowledge that Claims 8-13 are allowed.

Claims 3-4, 15, 19, 21 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants acknowledge these claims would be allowable if rewritten, as suggested. However, Applicants submit that the claims from which they depend should be allowable for the reasons stated above. Accordingly, Applicants respectfully request withdrawal of this objection.

Page 9

275256_1

PATENT

Infineon Dkt. No.: 2003PS2879US

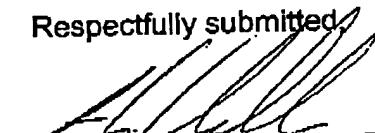
OC Docket No.: INFN/0026

CONCLUSION

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, Applicants believe that a detailed discussion of the secondary references is not necessary for a full and complete response to this office action.

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



Gero G. McClellan
Registration No. 44,227
MOSER, PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicant(s)